# A 6-18 GHz BROADBAND HIGH POWER MMIC FOR EW APPLICATIONS

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## ABSTRACT

A three stage, 6 - 18 GHz, dual channel MMIC power amplifier has been designed and tested. The design has been fabricated using a 0.25 μm T-gate, MBE grown GaAs-InGaAs-AlGaAs, power PHEMT process at Texas Instruments. The measured single channel small signal gain is 24.1 ± 3.4 dB over 6 - 18 GHz with an input return loss of >12 dB. The single channel output power at 2 dB gain compression, over 6 - 18 GHz is 3.4 ± 1.1 Watts pulsed and 2.4 ± 1.1 Watts CW. Using off chip combiners the dual channel amplifier gives 5.1 ± 1.3 Watts pulsed, 4.3 ± 1.3 Watts CW with a small signal gain of 24dB ± 3.5 dB over 6 - 18 GHz.

## 1 Introduction

Microwave solid state power amplifiers are attractive for EW applications because of their small size, low voltage operation, high intrinsic reliability and negligible warm up time. In many applications the system will require individual amplifiers to be combined into power modules which may then be deployed in phased arrays. MMIC technology is particularly suitable for the individual power amplifiers because it offers reduced and tightly controlled parasitic elements and largely eliminates wire bond interconnects. This enables broad operating bandwidths to be achieved at low cost, whilst good chip to chip repeatability and 50 Ω impedance allows power combination to be implemented more readily.

The amplifiers are typically combined into a power module using corporate or serial input power splitting and output power combining networks. These are commonly formed from building blocks such as Wilkinson dividers or Lange couplers. The upper limit to the number of amplifiers that can be efficiently combined is imposed by increasing transmission line losses and by increasingly stringent manufacturing tolerance requirements in the building blocks. Published work, for example Dicken et al (1), and our own unpublished work using alumina microstrip suggests a practical upper limit of order 8 to 16 amplifiers. It is therefore important to maximise the output power at the chip level and the work described in this paper addresses the design, fabrication and assessment of a high power broadband MMIC using an advanced GaAs PHEMT foundry process.

## 2 MMIC power amplifier design

Solid state power amplifier capability critically depends on the performance of the transistors, GaAs FET, PHEMT and HBT have all been used to design wide band power amplifiers. The highest reported output power level from a commercially available 6 - 18 GHz MMIC is 1.8 W and used HBT technology [2, 3]. The design target for the work reported in this paper was 5 Watt output power with >20 dB gain over 6 - 18 GHz. This is a very useful power level from a system point of view, it exceeds the current state of art, and it represented a challenging test of what can be achieved with advanced active device technology.

Our earlier work on power amplifier design using FET based technology [4] had indicated that a critical factor in achieving the wide band power specification would be the ability to maintain a sufficiently high gain per stage at the highest frequencies. This is so that the power amplifier output stage can always be driven into compression without the need for excessively large driver stages. Prioritisation of this criterion made a power

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PHEMT technology the choice for this work. For HBT technology the high frequency gain per stage can be lower but it does have a higher output power density and hence it may ultimately be the route to more powerful wideband MMIC amplifiers.

The specific MMIC process used for this work is a 0.25 μm power PHEMT process developed by Texas Instruments and accessed through the Texas foundry as an engineering process prior to full release. The process has an $f_t$ of 32GHz, provides devices with a typical gate drain breakdown of 16 to 18 volts and an output power density of ~ 0.7 Watts/mm.

The amplifier design was based on two 2.5 Watt channels on the same chip with external combiners to achieve the 5 Watt target. This architecture was chosen to allow greater flexibility in deploying the chips and to maximise the probability of success at the first iteration. For each channel, a three stage design was adopted to meet the 20 dB gain target. The first stage used a distributed amplifier topology to achieve a good input match over the design band and to provide positive gain slope compensation.

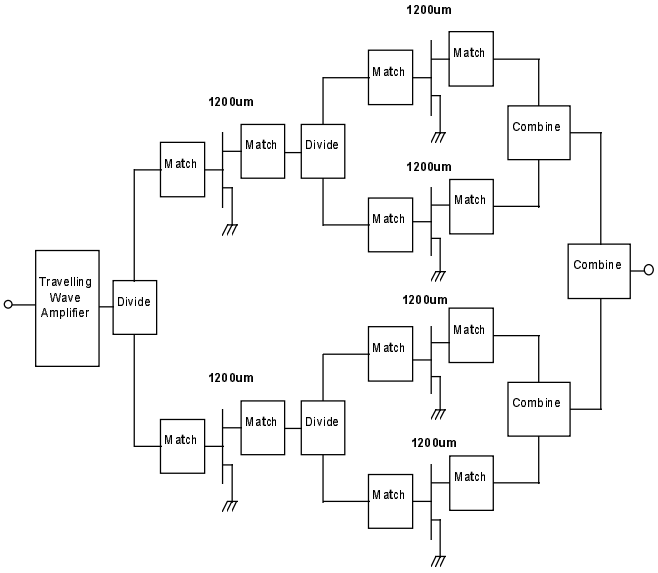


**Figure 1 : Simplified schematic for a single channel of the power amplifier**

The second stage used two 1200μm gate width transistors to drive an output stage consisting of four 1200μm transistors. A simplified circuit schematic is shown in figure 1.

Lossy matching techniques in the interstage network were used to provide additional gain slope compensation and provide the optimum impedance level for power matching. The output matching network was designed to present the optimum impedance to the four 1200μm transistors over the 6 - 18 GHz frequency band using experimental load pull data provided by Texas Instruments. Particular care was taken in selecting a matching network topology offering a good compromise between power match and low insertion loss. In this first iteration design no particular attempt was made to optimise the power added efficiency (PAE). Our previous power amplifier design work [4] had shown that to prevent the occurrence of odd mode oscillations it was necessary to connect small value resistors between the gate and drains of the large transistor cells. A linear and non-linear CAD package[1] was used for the circuit simulation and design, and electromagnetic simulation software was additionally employed for the detailed design of the matching networks[2].

A photograph of the dual-channel power amplifier is shown in figure 2, the circuit size is 6.9 x 5.9 $mm^2$. The input and output ports of both channels were arranged to have a separation of approximately 3 mm so that they were compatible with Lange coupler dimensions on 0.015" alumina. Test structures were also included on the mask set so that the distributed amplifier and output amplifier stage could be measured in isolation for diagnostic purposes.

## 3 Measurement

Three wafers containing the power amplifier MMIC were manufactured. Each circuit was tested for dc functionality and a dc yield was obtained which varied between 75% and 85%. Initially, RFOW probe measurements of small signal gain and return loss were made on the individual channels under CW conditions. Figure 3 shows the measured and simulated small signal gain and input return loss for a single channel.

[1] Libra HP-Eesof
[2] EM Sonnet Software Inc., Liverpool, NY

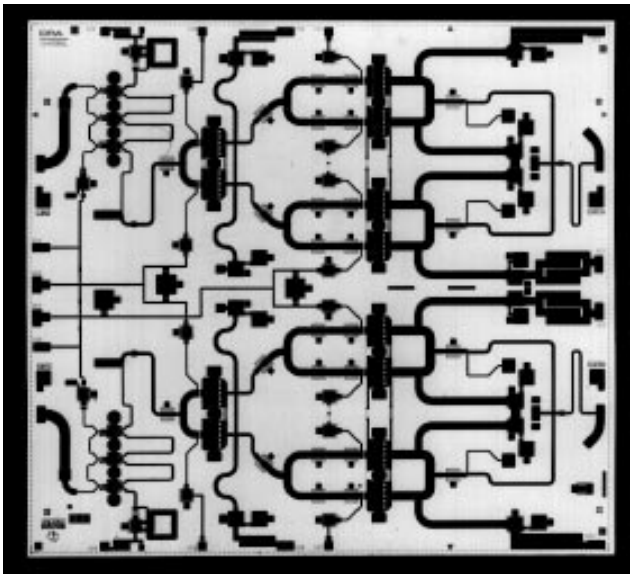

**Figure 2 : Photograph of power MMIC**

The measured gain is 26 dB at 6 GHz falling to 18 dB at 18 GHz, input return loss is better than 12 dB over the design band. For power measurements the chip was soldered on to a silvar carrier and mounted into a coaxial test jig using Wiltron 'K' connectors. The chip was interfaced with 7 mm long 50 Ω microstrip lines on 0.015" alumina.

Some test jig heat sinking was incorporated but the thermal design had not been optimised, hence the initial measurements were made under both CW and pulsed conditions, the latter using a 1 ms pulse width with a 20 ms period. The drain supply voltage, measured at the chip, was 8 volts for all of the results reported here. Small signal gain and output power over the 5 - 19 GHz frequency range for a single amplifier channel, are shown in figure 4 for CW and pulsed conditions respectively.

The single channel output power at 2 dB gain compression from 6 - 18 GHz was greater than 31.3 dBm for CW operation and 33.7 dBm for pulse operation, the maximum CW and pulse output powers were 35.5 and 36.5 dBm respectively at 8 and 13 GHz, as shown in figure 4. These measurements are corrected for test jig losses.

Lange couplers on 0.015" alumina were used to combine the output from the two MMIC amplifier channels. Measured small signal gain and output power at 2 dB gain compression for the combined amplifier under both CW and pulsed conditions are shown in figure 5. The pulsed output power over 6 - 18 GHz was greater than 35.7 dBm with a peak value of 38.4 dBm, the CW output power was greater than 34.7 dBm with a peak of 37.5 dBm.

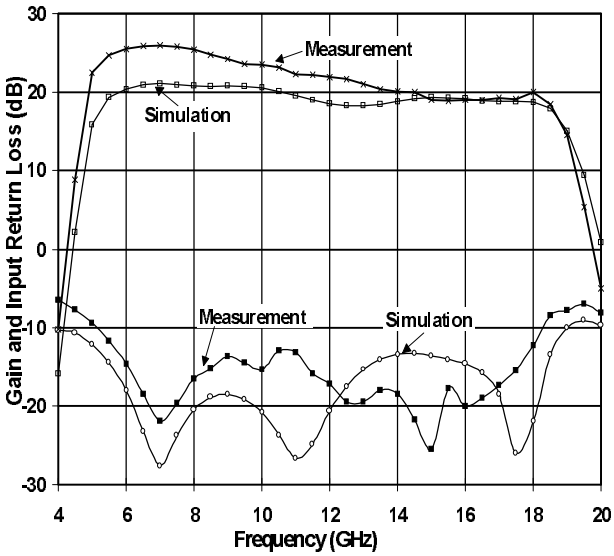


**Figure 3 : Measured and modelled small signal response for a single channel.**

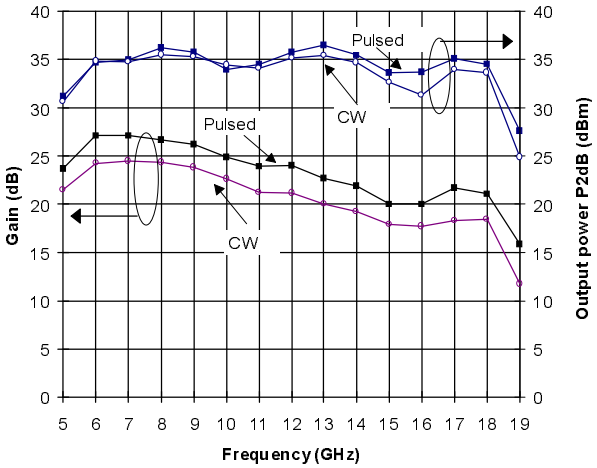


**Figure 4: Gain and output power for a single channel**

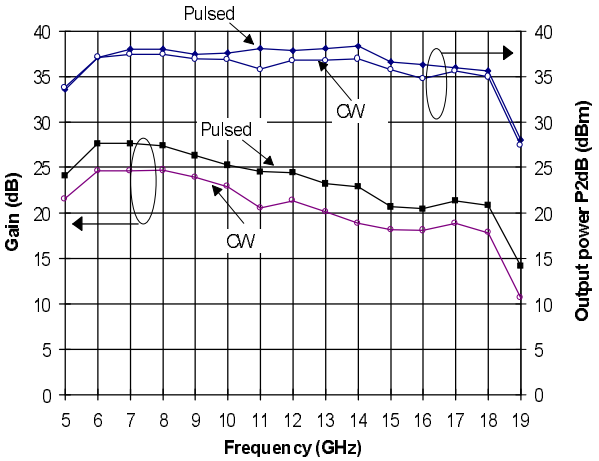


**Figure 5: Gain and output power for combined channels**

The power added efficiency of the single and combined amplifier has been measured under CW conditions. The PAE is between 10% and 30% for the single channel and 12% and 27% for the balanced amplifier. Over 6-14GHz the PAE was typically better than 20%.

## 4 Conclusion

A GaAs PHEMT MMIC power amplifier covering 6 - 18GHz has been designed and fabricated and initial assessment measurements made. The single channel output power at 2 dB gain compression over 6 - 18 GHz is 3.4 ± 1.1 Watts pulsed and 2.4 Watts ± 1.1 Watts CW. The dual channel amplifier gives 5.1 ± 1.3 Watts pulsed, 4.3 ± 1.3 Watts CW with a small signal gain of 24dB ± 3.5 dB over 6 - 18 GHz. A power of > 5 Watts was achieved pulsed over 6 - 14 GHz with > 3.8 Watts CW. We believe these are the highest wideband power results reported for MMIC amplifiers.

The Lange couplers combining the two amplifier channels are strongly overcoupled to achieve operation over the 6 - 18 GHz band and it is clear from the measurements that the combining efficiency decreases towards 18 GHz. This has reduced both the high frequency power and the PAE. Additional power measurements are planned using more effective combining structures and heatsinking with the expectation that the output power capability indicated by the single channel pulsed measurements will be realisable CW across the full design bandwidth.

These results are important because they demonstrate that PHEMT based high power MMICs can achieve powers of > 5 Watts over 6 - 18 GHz with high gain, and high yield. Such power levels, combined with the benefits of small size, low voltage operation, high intrinsic reliability, negligible warm up time and the flexibility of wide band phased arrays make this a viable and important component technology for deployment in solid state EW systems. The peak PAE of 30% is particularly important for array applications where prime power and cooling requirements will be critical considerations - further work is planned to increase the output power level and PAE.

## 5 Acknowledgements

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## 6 References

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